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(56) Documents Cited

EP 0337109 A GB 2289984 A

WO 99/16118 A

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(54) Abstract Title Method of fabricating a semiconductor device

(57) A method for fabricating a semiconductor device, including the steps of: forming a contact hole (208, Figure 2c) so as to cause the etching stopper 205 on the substrate 201 to be exposed; removing an exposed etching stopper 205 on the substrate; filling the contact hole 208 to form a contact plug 210; removing a film [209, Figure 3b] that is deposited on the interlayer insulation film 206, so as to expose the contact plug 210; etching the interlayer insulation film 206 and removing the etching stopper 205 on the gate electrode 203; forming an interlayer insulation film 211; etching the interlayer insulation film 211 so as to expose the etching stopper 205 on a diffusion layer [231, Figure 5a] and etching the insulation film 204 of the gate electrode 203, so as to form contact holes [213, Figure 5a] on the diffusion layer 231 and gate electrode 203; removing the etching stopper 205 exposed on the diffusion layer 231; and, filling the contact hole 213, so as to form the contact plugs 215.

Fig. 6

